WHAT IS CLAIMED IS:

1. A packaged semiconductor, comprising:

a leadframe comprising at least two groups of a plurality of leads wherein each one of said plurality of leads has an upper side, a lower exposed side, and a laterally exposed side, the upper side of said each one of said plurality of leads defining a generally co-planar surface with the upper side of a first group of said at least two groups of a plurality of leads;

a semiconductor chip placed above the generally co-planar surface defined by the upper side of said first group of said at least some of said plurality of leads;

a plurality of electrical connectors electrically connecting said semiconductor chip to a second group of said at least two groups of a plurality of leads; and

sealing material encapsulating said leadframe, said semiconductor chip, and said plurality of electrical connectors, said lower exposed side and said laterally exposed side of at least one of said plurality of leads resting flush with a bottom surface of said semiconductor package and a side surface of said semiconductor package.

2. The semiconductor package of claim 1 wherein said leadframe has a paddle for supporting said semiconductor chip, said paddle having a top side and a bottom side, said top side located in the generally co-planar surface of said leadframe.

3. The semiconductor package of claim 1 wherein said electrical connectors comprise a plurality of wires.

4. The semiconductor package of claim 3 wherein said plurality of wires are selected from a material in the group consisting of: gold, silver, aluminum, or a combination thereof.

5. The semiconductor package of claim 1 wherein said electrical connectors are a plurality of solder balls.

6. The semiconductor package of claim 1 wherein said leadframe is made of copper.

7. The semiconductor package of claim 1 wherein said lower exposed side is plated with a corrosion-minimizing material.

8. The semiconductor package of claim 7 wherein said corrosion-minimizing material is selected from the group comprised of tin, gold, tin lead, nickel palladium, tin bismuth, or a combination thereof.

9. A leadframe, comprising:

a plurality of leads, each one of said plurality of leads has an upper side and a lower exposed side, said upper side of said each one of said plurality of leads forming a generally co-planar surface with said upper side of at least some of said plurality of leads, each one of said plurality of leads has an outwardly extending portion; and

a tie bar connected to said outwardly extending portion of said plurality of leads configured so that when said tie bar is trimmed off said leadframe during the semiconductor packaging process, said trimming off of said plurality of leads leaves a laterally exposed surface of said plurality of leads.

10. The leadframe of claim 9 further comprising a paddle, said paddle having a top side located in said generally co-planar surface.

11. The leadframe of claim 9 wherein said leadframe is copper.

12. A semiconductor package, comprising:

a leadframe comprising at least two groups of a plurality of leads wherein each one of said plurality of leads has an upper side, a lower exposed side, and a laterally exposed side, the upper side of said each one of said plurality of leads defining a generally co-planar surface with the upper side of a first group of said at least two groups of a plurality of leads, said generally co-planar surface of said leadframe for attaching to a semiconductor chip;

a plurality of electrical connectors electrically connecting said semiconductor chip to a second group of said at least two groups of a plurality of leads; and

sealing material encapsulating said leadframe, said semiconductor chip, and said plurality of electrical connectors, said lower exposed side and said laterally exposed side of said plurality of leads resting flush with a bottom surface of said semiconductor package and a side surface of said semiconductor package.

13. A method for manufacturing a packaged semiconductor, comprising the steps:

attaching a semiconductor chip to a leadframe, said leadframe comprising at least two groups of a plurality of leads wherein each one of said plurality of leads has an upper side and a lower exposed side, the upper side of said each one of said plurality of leads defining a generally co-planar surface with the upper side of a first group of said at least

two groups of a plurality of leads, said semiconductor chip attached to the generally co-planar surface defined by the upper side of said first group of said at least some of said plurality of leads;

electrically connecting a plurality of electrical connectors on said semiconductor chip to a second group of said at least two groups of a plurality of leads;

encapsulating said leadframe, said semiconductor chip, and said plurality of electrical connectors with a sealing material, said lower exposed side resting flush with a bottom surface of said semiconductor package; and

trimming off excess encapsulant and a portion of said leadframe to expose a lateral side of said plurality of leads, said lateral side of at least one lead of said plurality of leads resting flush with a side surface of said semiconductor package.